

FIG. 1

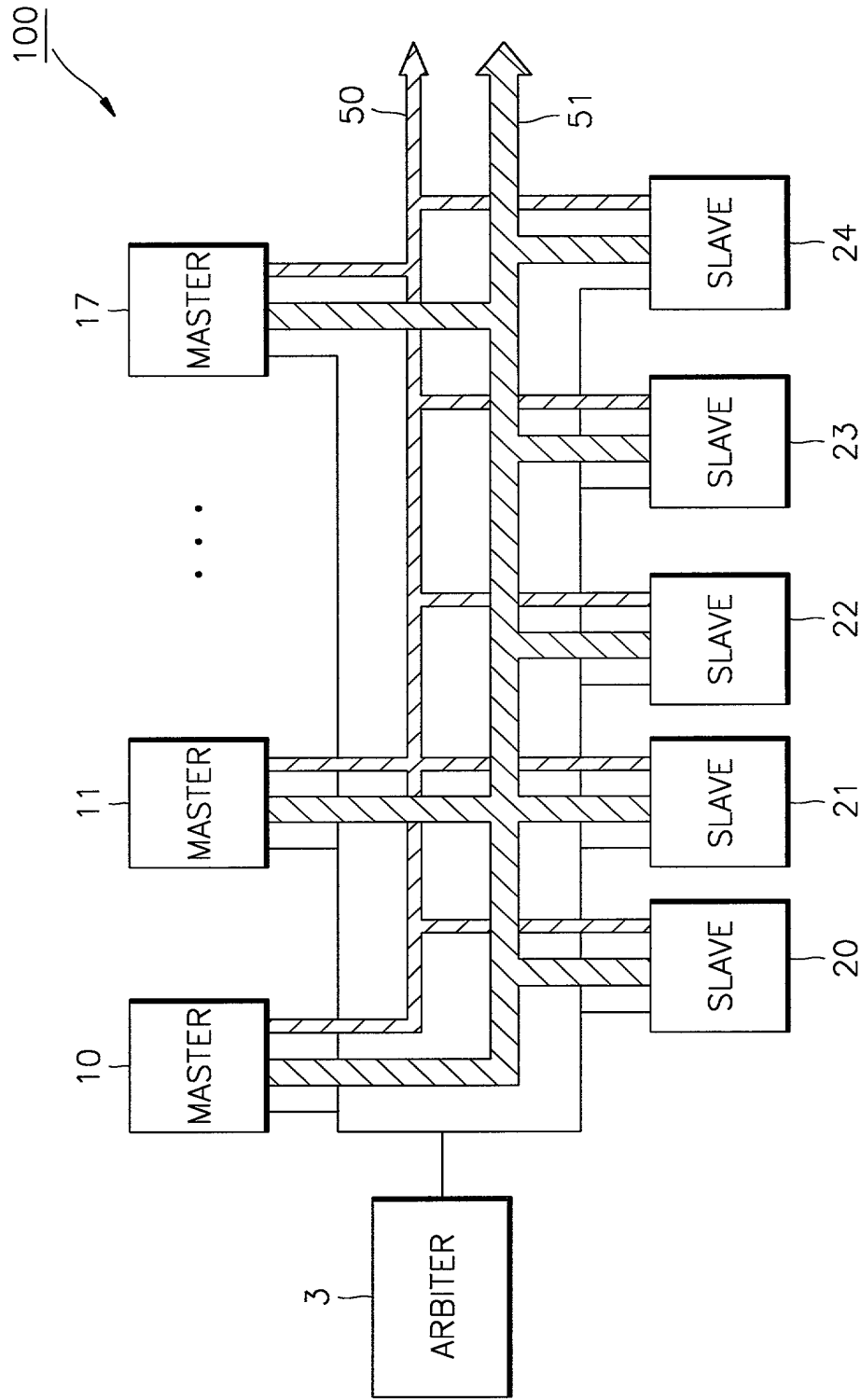


FIG. 2

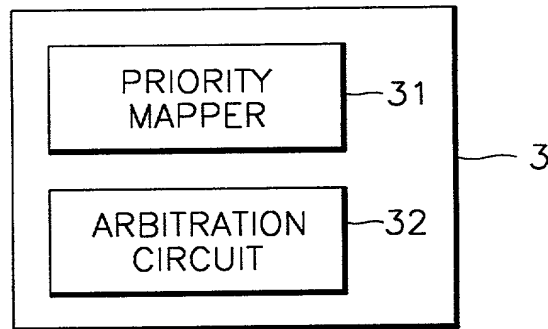


FIG. 4

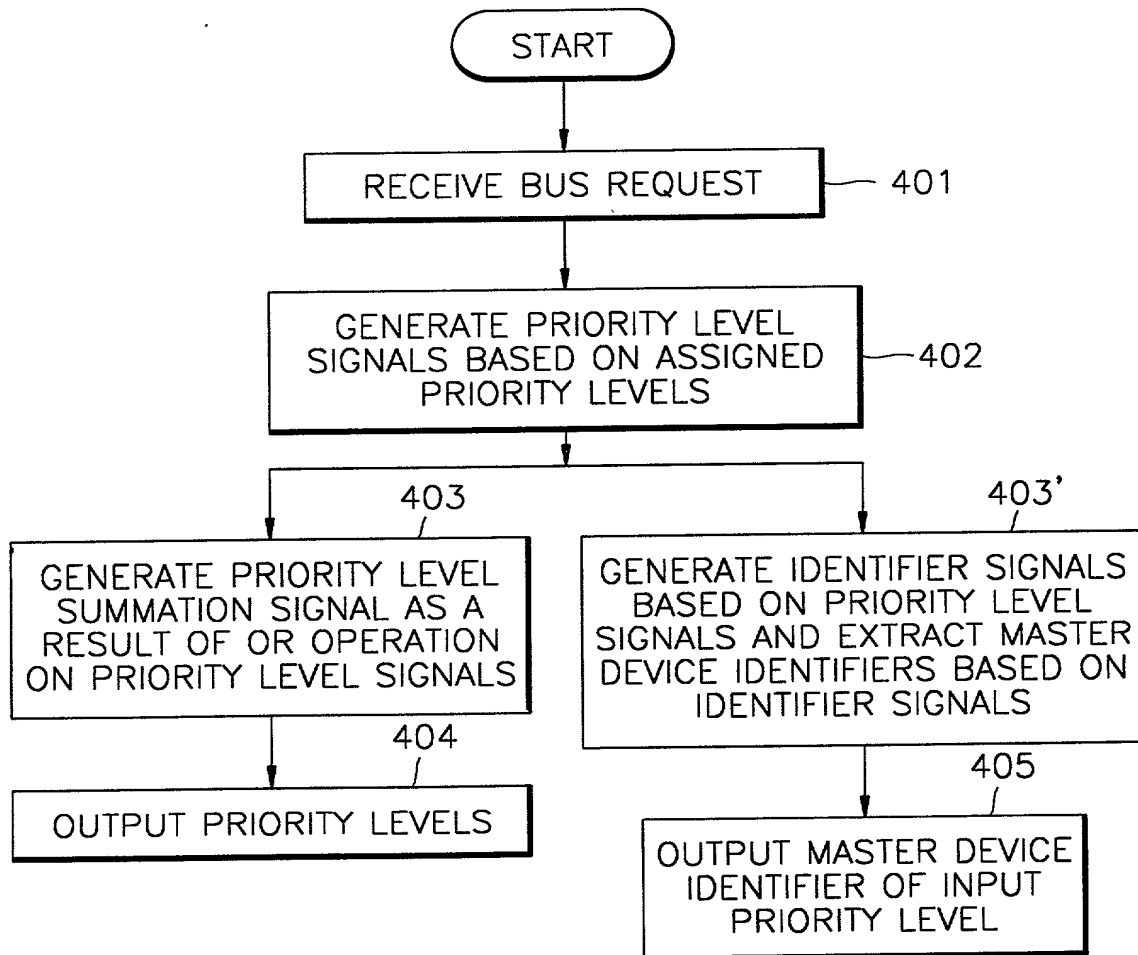


Figure 1 is a block diagram of a master ID assignment circuit. The circuit is divided into two main sections: the upper section (300) for priority assignment and the lower section (302) for identifier assignment. Both sections have 8 masters (MASTER 0 to MASTER 7) and 16 registers (REGISTER 0 to REGISTER 7). In the upper section, each register is connected to an OR OPERATOR (0 to 15), which then feeds into a PRIORITY OUTPUT UNIT (301). The lower section has a similar structure with DECODER (0 to 15) units feeding into an IDENTIFIER OUTPUT UNIT (303). A MASTER ID input is shown at the bottom.